library IEEE;

use IEEE.STD\_LOGIC\_1164.all;

entity Comparator\_structural is

port(

a : in BIT;

b : in BIT;

c : in BIT;

d : in BIT;

f1 : out BIT;

f2 : out BIT;

f3 : out BIT

);

end Comparator\_structural;

--}} End of automatically maintained section

architecture Arhitectura of Comparator\_structural is

component INVERSOR is

port (a : in bit;

y : out bit);

end component INVERSOR;

component COINCIDENTA is

port (a,b : in bit;

y : out bit);

end component COINCIDENTA;

component OR\_3 is

port(a,b,c : in bit;

y : out bit);

end component OR\_3;

component AND\_2 is

port (a,b : in bit;

y : out bit);

end component AND\_2;

component AND\_3 is

port (a,b,c : in bit;

y : out bit);

end component AND\_3;

signal f11,f12:bit;

signal f21,f22,f23:bit;

signal f31,f32,f33:bit;

signal nota,notb,notc,notd:bit;

begin

-- enter your statements here --

u1:coincidenta port map(a,c,f11);

u2:coincidenta port map(b,d,f12);

u3:and\_2 port map(f11,f12,f1);

i1:inversor port map(a,nota);

i2:inversor port map(b,notb);

i3:inversor port map(c,notc);

i4:inversor port map(d,notd);

v1:and\_3 port map(nota,notb,d,f21);

v2:and\_3 port map(notb,c,d,f22);

v3:and\_2 port map(nota,c,f23);

v4:or\_3 port map(f21,f22,f23,f2);

t1:and\_2 port map(a,notc,f31);

t2:and\_3 port map(a,b,notd,f32);

t3:and\_3 port map(b,notc,notd,f33);

t4:or\_3 port map(f31,f32,f33,f3);

end Arhitectura;